LISTING OF CLAIMS

1. (Currently Amended) A method for the synchronous transmission of an n-bit binary signal ~~signals~~ through a bus of m leads, where m<n, comprising ~~characterized in that it comprises the following operations~~:

compressing the n-bit binary signal ~~signals~~ to be transmitted in such a way as to reduce its ~~their~~ number of bits to an m-bit binary signal, and

decompressing the m-bit binary signal ~~signals thus~~ transmitted through the bus until its number of bits ~~their number~~ is again equal to the n-bit number of the n-bit binary signal prior to the compressing ~~encoding~~.

2. (Currently Amended) A ~~The~~ method ~~in accordance with Claim 1,~~ for the synchronous transmission of n binary signals through a bus of m leads, where m<n, comprising:

compressing the signals to be transmitted in such a way as to reduce its number of signals, wherein compressing comprises choosing, from among the signals to be transmitted, a first and a second signal and encoding of the first signal on the second signal in order to obtain an encoded signal; and

decompressing the signals transmitted through the bus until their number of signals is again equal to the number of signals prior to the encoding, wherein decompressing comprises decoding of the encoded signal in order to obtain a first and a second output signal that reproduce, respectively, the first and the second signal.

3. (Original) The method in accordance with Claim 2, wherein, from among the leading edge and the trailing edge of a train of clock pulses, there is chosen one edge as the reading edge of the signals, and wherein encoding provides for the information associated with the first signal to be included in the second signal within a predetermined time interval of the clock period preceding each reading clock pulse.

4. (Original) The method in accordance with Claim 3, wherein the encoding comprises the following operations:

monitoring the first signal and the second signal to ascertain whether their state does or does not change between two successive clock pulses,

generating the encoded signal according to the following criterion:

when the first signal does not change during the clock period preceding the reading clock pulse, the encoded signal is equal to the second signal delayed by one clock period,

when the first signal changes during the clock period preceding the reading clock pulse, the encoded signal is a signal that differs from the second signal by the fact that it is inverted in the predetermined time interval of the clock period preceding every reading clock pulse when the second signal has not changed in the clock period preceding the reading clock pulse, otherwise, when the second signal has changed in the clock period preceding the reading clock pulse, it remains equal to the second signal in the same predetermined time interval,

and wherein the decoding comprises the following operations:

reading the encoded signal coming from the lead of the transmission bus on the reading edge of the clock pulse following the one which the encoding was effected and sending it as first output signal to a first output terminal,

monitoring the encoded signal to ascertain whether its state has or has not changed in the predetermined time interval and

reconstructing the first signal as second output signal at a second output terminal, inverting or not inverting the second output signal as it was in the clock period preceding the reading clock pulse according to the state ascertained in the preceding operation.

5. (Original) The method in accordance with Claim 3, wherein there are chosen a first signal, a second signal and a third signal in order to obtain a first encoded signal and a second encoded signal and wherein the encoding comprises the following operations:

monitoring the first, the second and the third signal to ascertain whether their state does or does not change between two successive clock pulses,

generating the first encoded signal and the second encoded signal in accordance with the following criterion:

when the first signal has not changed in the clock period preceding the reading clock pulse, the first encoded signal and the second encoded signal are equal to, respectively, the second signal and the third signal delayed by one clock period,

when the first signal has changed in the clock period preceding the reading clock pulse,

the second encoded signal is equal to the third signal read in a predetermined time interval in the clock period preceding the reading clock pulse and

the first encoded signal is the inverse of the second signal read in the predetermined time interval when the second signal and the third signal have not changed in the clock period preceding the reading clock pulse, otherwise it is equal to the second signal read in the predetermined time interval and

wherein the encoding comprises the following operations:

reading the first encoded signal and the second encoded signal arriving from the transmission bus on the reading edge of the clock pulse following the one in which the encoding was effected and sending them, respectively, to a first and a second output terminal as first and second output signal,

monitoring the first and the second encoded signal to ascertain whether their state has or has not changed in the predetermined time interval and

reconstructing the first signal as second output signal on a second output terminal by not inverting the second output signal as it was in the clock period preceding the reading clock pulse when neither the second nor the third signal has changed after the previous operation or inserting it when at least one of the second and the third signal has changed.

6. (Currently Amended) A circuit system for the synchronous transmission on a bus of m leads of n binary signals, where m<n, comprising a clock pulse generator, an encoder and a decoder, wherein:

the encoder comprises:

a multiplicity of input terminals capable of receiving the n signals, including at least a first and a second signal selected for encoding the first signal on the second signal, at least one output terminal connected to a lead of the bus to transmit an encoded signal and first logic means capable of:

monitoring the first signal and the second signal in order to ascertain whether their state does or does not change between two successive clock pulses,

generating the encoded signal in accordance with the following criterion:

when the first signal has not changed in the clock period preceding the reading clock pulse, the encoded signal is equal to the second signal delayed by one clock period, and

when the first signal has changed in the clock period preceding the reading clock pulse, the encoded signal is a signal that differs from the second signal by the fact that, in the predetermined time interval of the clock period preceding every reading clock pulse, it is inverted when the second signal has not changed or has changed in the clock period preceding the reading clock pulse, otherwise, when the second signal has changed in the clock period preceding the reading clock pulse, in the same predetermined time interval it remains equal to the second signal, and

the decoder comprises at least one input terminal connected to a lead of the bus to receive an encoded signal, a multiplicity of output terminals, including at least two terminals for two output signals corresponding to the first and the second signal selected for encoding and logic means capable of:

reading the encoded signal arriving from the lead of the transmission bus on the reading edge of clock pulse following the clock pulse during which the encoding was effected and sending it as first output signal to a first output terminal,

monitoring the encoded signal to ascertain whether its state has or has not changed during the predetermined time interval, and

reconstructing the first signal as second output signal at a second output terminal, inverting or not inverting the second output signal in the clock period preceding the reading clock pulse in accordance with the state ascertained by the previous operation.

7. (Original) A method for encoding a first digital signal onto a second digital signal, comprising:

generating an output signal having a state at a given clock signal edge which matches a state of the second digital signal and having a transition or not in state occurring in a time period preceding the given clock signal edge that is indicative of a state of the first digital signal.

8. (Original) The method according to Claim 7, wherein the given clock signal edge is a leading edge and the time period preceding is an interval between a leading and trailing edges of a preceding clock pulse.

9. (Original) The method according to Claim 7, wherein the output signal state at the given clock signal edge is the state of the second digital signal delayed by one clock period and any transition in the output signal during the time period preceding the given clock signal edge indicates a change in state of the first digital signal.

10. (Original) The method according to Claim 7, wherein generating comprises:

setting the output signal state equal to the second signal delayed by one clock period when the first signal does not change state during the time period preceding the given clock signal edge;

transitioning the output signal state during the time period preceding the given clock signal edge when the first signal changes state during the clock period preceding the reading clock pulse.

11. (Original) The method according to Claim 10, wherein transitioning comprises setting the output signal state to be inverted in the time period preceding the clock signal edge when the second signal has not changed state in the time period preceding the clock signal edge, and otherwise setting the output signal state to equal the second signal in the time period preceding the clock signal edge when the second signal has changed in the clock period preceding the reading clock pulse.

12. (Original) A method for decoding an encoded digital signal, comprising:

generating a first output signal having a state at a given clock signal edge which matches a state of the encoded digital signal; and

generating a second output signal having a state having a state that is indicated by a transition or not in state of the encoded digital signal which occurs in a time period preceding the given clock signal edge.

13. (Original) The method according to Claim 12, wherein the given clock signal edge is a leading edge and the time period preceding is an interval between a leading and trailing edges of a preceding clock pulse.

14. (Original) The method according to Claim 12, wherein the steps of generating comprise:

reading the encoded digital signal at the given clock signal edge to generate the first output signal;

monitoring the encoded digital signal to determine whether its state changed during the time period preceding the given clock signal edge; and

producing the second output signal through selective inverting thereof in accordance with the monitored state change.

15. (Original) An encoder for encoding a first digital signal onto a second digital signal, comprising:

a first circuit that controls a state of an output digital to match a state of the second digital signal at a given clock signal edge; and

a second circuit that controls the state of the output digital signal to transition or not during a time period preceding the given clock signal edge in a manner which is indicative of a state of the first digital signal .

16. (Original) The encoder according to Claim 15, wherein the given clock signal edge is a leading edge and the time period preceding is an interval between a leading and trailing edges of a preceding clock pulse.

17. (Original) The encoder according to Claim 15, wherein the output signal state at the given clock signal edge is the state of the second digital signal delayed by one clock period and any transition in the output signal during the time period preceding the given clock signal edge indicates a change in state of the first digital signal.

18. (Original) The encoder according to Claim 15, wherein:

the first circuit sets the output signal state equal to the second signal delayed by one clock period when the first signal does not change state during the time period preceding the given clock signal edge; and

the second circuit transitions the output signal state during the time period preceding the given clock signal edge when the first signal changes state during the clock period preceding the reading clock pulse.

19. (Original) A decoder for decoding an encoded digital signal, comprising:

a first circuit that generates a first output signal having a state at a given clock signal edge which matches a state of the encoded digital signal; and

a second circuit that generates a second output signal having a state having a state that is indicated by a transition or not in state of the encoded digital signal which occurs in a time period preceding the given clock signal edge.

20. (Original) The decoder according to Claim 19, wherein the given clock signal edge is a leading edge and the time period preceding is an interval between a leading and trailing edges of a preceding clock pulse.

21. (Original) The decoder according to Claim 19,

wherein the first circuit reads the encoded digital signal at the given clock signal edge to generate the first output signal; and

wherein the second circuit monitors the encoded digital signal to determine whether its state changed during the time period preceding the given clock signal edge, and produces the second output signal through selective inverting thereof in accordance with the monitored state change.